UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,496	09/23/2003	Xin Chang	372465-01401	3986

37509 7590 04/06/2005

DECHERT LLP
P.O. BOX 10004
PALO ALTO, CA 94303

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,496	CHANG ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/669,496 filed on 9/23/2003. Claims 1-7 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4-5 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Pacific et al. (6,550,044).

4. As to claims 1, 5 and 7, Pavisic et al. teach a method of resolving timing violations in a network of components and interconnects for a physical of an IC comprising performing a timing analysis on the network, one or more components or interconnects of the network, each having a particular amount of timing potential; and performing a selective in-place optimization by identifying components or interconnects of the network that have the highest amount of timing violation potential and executing an in place optimization according to the identified components or interconnects (see

abstract, summary, Fig. 1-5 and its description, at least col. 2, lines 28-67, col. 3, lines 1-8).

5. As to claim 4, Pavisic et al. teach in-place optimization is performed including buffer optimization, gate resizing (down sizing the components, up sizing the components), and logic restructuring.

6. Claims 1, 4-5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Graef et al. (6,189,131).

7. As to claims 1, 5 and 7, Graef et al. teach a method of resolving timing violations in a network of components and interconnects for a physical of an IC comprising performing a timing analysis on the network, one or more components or interconnects of the network, each having a particular amount of timing potential; and performing a selective in-place optimization by identifying components or interconnects of the network that have the highest amount of timing violation potential and executing an in place optimization according to the identified components or interconnects (see abstract, summary, Fig. 1-5 and its description, col. 5, line 32 to col. 8 line 13).

8. As to claim 4, Graef et al. teach in-place optimization is performed more substantial changes using additional path restructuring capabilities in the post layout optimization to generate floorplanning and synthesis information in form of an SDF file/RC (design exchange file; resistance and capacitance). This information is communicated to synthesis and floorplanning tools. Once any necessary or desirable changes have been made by the synthesis tools, the changes are communicated back

to the floorplanning tools in the form of PDEF (physical design exchange file) information.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2-3 and 6 are rejected under 35 U.S.C. 103(a) as being obvious over Pavisic et al. (6,550,044) in view of Hathaway et al. (5,963,728) and Graef et al. (6,189,131) and further view of Arnold et al. (6,099,584).

11. As to claims 2 and 6, Pavisic et al. teach examples of user-provided criteria (col. 3 lines 13-41). Hathaway et al. teach a method of designing a clock network according to user criteria (see abstract, summary, each clock net is than a maximum load criteria or net cap or net load, load sink), where adding and removing of clock nets is performed in order to meet these criteria. Graef et al. teach a method of selecting and synthesizing metal interconnect wires in IC design by providing user-criteria including cell delay, transition times (transition delays), net cap and interconnect delays for use by static timing analysis in in-place optimization (Fig. 3-4, summary, col. 4, col. 5, lines 32-67, col. 6, lines 1-25; col. 7 lines 1-67, col. 8 lines 1-12). Arnold et al. teach a method for resolving timing violations in an IC design including providing timing reports for use by in-place optimization in order to verify timing to meet timing criteria or timing criteria

(Fig. 4-6 and description). By combining these above teachings, it would have been obvious to one of ordinary skill in the art at the time the invention was made claimed limitations as recited because the user-criteria provided, generated reports, and removal of clock nets as taught in above rejection would have been provided to static timing analysis and placement and routing, thereby the in-place optimization would have been performed to correct any timing violations and other signal integrity problems detected by the static timing analysis. Using these above static timing analysis and in-place optimization allows designers to perform minimal design changes and/or substantial changes of an IC design. Once any necessary or desired changes have been made, the changes are communicated back (reports) to the placement and routing in order to refine the IC design in order to correct any timing violations to meet the user-provided criteria.

12. As to claim 3, Graef et al. teach storing timing related information in a Net File (at least in col. 6, lines 39-67, SDF, DEF, PDEF, wire layer attribute file) for use by static timing analysis, synthesis and layout tools in order to perform in-place optimization to correct timing violations to meet user-provided criteria (design constraints provided).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER